PDF SOLUTIONS INC
Form 10-K
March 15, 2012

UNITED STATES SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

Form 10-K

(Mark One)

R	ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 For the fiscal year ended December 31, 2011
	or
£	TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 For the transition period from to

000-31311
(Commission file number)

PDF SOLUTIONS, INC.
(Exact name of registrant as specified in its charter)

Delaware (State or other jurisdiction of Incorporation or organization)	25-1701361 (I.R.S. Employer Identification No.)
333 West San Carlos Street, Suite 700 San Jose, California (Address of Registrant's principal executive offices)	95110 (Zip Code)

(408) 280-7900
(Registrant's telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of Class	Name of Each Exchange on Which Registered
Common Stock, $0.00015 par value	The NASDAQ Stock Market LLC

Securities registered pursuant to Section 12(g) of the Act:
None

Indicate by check mark if the registrant is a well-known seasoned issuer (as defined in Rule 405 of the Securities Act). Yes £ No R

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes £ No R

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes R No £

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§ 232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes R No £

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. o

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer £ Accelerated filer R Non-accelerated filer £ Smaller reporting company £
(Do not check if a smaller reporting company)

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes £ No R

The aggregate market value of the voting stock held by non-affiliates of the Registrant was approximately $121.9 million as of the last business day of the Registrant's most recently completed second quarter, based upon the closing sale price on the NASDAQ Global Market reported for such date. Shares of Common Stock held by each officer and director and by each person who owns 10% or more of the outstanding Common Stock have been excluded in that such persons may be deemed to be affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

There were 28,464,040 shares of the Registrant's Common Stock outstanding as of March 5, 2012.

DOCUMENTS INCORPORATED BY REFERENCE

Part III incorporates certain information by reference from the definitive Proxy Statement to be filed within 120 days from December 31, 2011.

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PART I

This Annual Report on Form 10-K, particularly in Item 1 "Business" and Item 7 "Management's Discussion and Analysis of Financial Condition and Results of Operations," includes forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 (the "Securities Act") and Section 21E of the Securities Exchange Act of 1934, as amended (the "Exchange Act"). These statements include, but are not limited to, statements concerning: expectations about the effectiveness of our business and technology strategies; expectations regarding stock market and global economic trends; expectations regarding previous and future acquisitions; current semiconductor industry trends; expectations of the success and market acceptance of our intellectual property and our solutions; expectations that our cash, cash equivalents and cash generated from operations will satisfy our business requirements for the next twelve months; expectations of our future liquidity requirements; and our ability to obtain additional financing when needed. Our actual results could differ materially from those projected in the forward-looking statements as a result of a number of factors, risks and uncertainties discussed in this Form 10-K, especially those contained in Item 1A of this Form 10-K. The words "may," "anticipate," "plan," "continue," "could," "projected," "expect," "believe," "intend," and " negative of these terms and similar expressions are used to identify forward-looking statements. All forward-looking statements and information included herein is given as of the filing date of this Form 10-K with the Securities and Exchange Commission ("SEC") and based on information available to us at the time of this report and future events or circumstances could differ significantly from these forward-looking statements. Unless required by law, we undertake no obligation to update publicly any such forward-looking statements.

The following information should be read in conjunction with the Consolidated Financial Statements and notes thereto included in this Annual Report on Form 10-K. All references to fiscal year apply to our fiscal year that ends on December 31.

Item 1. Business

Business Overview

PDF Solutions is a leading provider of infrastructure technologies and services to lower the cost of integrated circuit ("IC") design and manufacturing, enhance time to market, and improve profitability by addressing design and manufacturing interactions from technology development and product design to initial process ramps to mature manufacturing operations. Our technologies and services target the entire "process life cycle," which is the term we have coined for the time from technology development and the design of an IC through volume manufacturing of that IC. Our solutions combine proprietary software, physical intellectual property in the form of cell libraries for IC designs, test chips, an electrical wafer test system, proven methodologies, and professional services. We analyze yield loss mechanisms to identify, quantify, and correct the issues that cause yield loss. Our analysis drives IC design and manufacturing improvements to enable our customers to optimize the technology development process, to increase initial yield when an IC design first enters a manufacturing line, to increase the rate at which yield improves, and to minimize excursions and process variability that cause yield loss throughout mass production. The result of successfully implementing our solutions is the creation of value that can be measured based on improvements to our customers' actual yield. Through our gainshare performance incentives component, we have aligned our financial interests with the yield and performance improvements realized by our customers, and we receive revenue based on this value. Our technologies and services have been sold to leading integrated device manufacturers, fabless semiconductor companies, and foundries.

The key benefits of our solutions to our customers are:

Faster Time to Market. Our solutions are designed to accelerate our customers' time-to-market and increase product profitability. Our solutions, which can predict and improve product yield even before IC product design is complete, transform the traditional design-to-silicon sequence into a primarily concurrent process, thereby shortening our customers' time-to-market. Systematically incorporating knowledge of the integration of the design and manufacturing processes into our software modules and physical IP enables our customers to introduce products with higher initial yields faster. Our solutions are designed to decrease design and process iterations and reduce our customers' up-front costs, and thus provide our customers with early-mover advantages such as increased market share and higher selling prices.

Faster Time to Volume. After achieving higher initial yields and faster time-to-market, our solutions are designed to enable our customers to isolate and eliminate remaining yield issues to achieve cost efficient volume manufacturing. Once a manufacturing process has been modeled using our solutions, our customers are able to diagnose problems and simulate potential corrections more quickly than using traditional methods. In addition, if process changes are required, improvements can be verified more quickly using our technology than using traditional methods. Our solutions thus enable our customers to quickly reach cost efficient volume, so that they are able to increase margins, improve their competitive position, and capture higher market share.

Increased Manufacturing Efficiencies. Our solutions for product design, product introduction, yield ramp, and process control are designed to allow our customers to achieve a higher yield at mass production and therefore a lower cost of goods sold. In addition, our solutions, which also include fault detection and classification ("FDC") software, are designed to provide our customers with the ability to proactively monitor process health to avoid potential yield problems.

Our long-term business objective is to maximize IC yield by providing the industry standard in technologies and services for the Process Life Cycle. To achieve this objective, we intend to:

Extend Our Technology Leadership Position. We intend to extend our technology leadership position by leveraging our experienced engineering staff and codifying the knowledge that we acquire in our solution implementations. For example, we continue to expand and develop new technology that leverages our Characterization Vehicle® (CV®) methodology to embed test structures on product wafers. This provides valuable insight regarding product yield loss during mass production with minimal or no increase in test time and non-product wafers. In addition, we selectively acquire complementary businesses and technologies to increase the scope of our solutions.

Leverage Our Gainshare Performance Incentives Business Model. We intend to continue expanding the gainshare performance incentives component of our customer contracts. We believe this approach allows us to form collaborative and longer-term relationships with our customers by aligning our financial success with that of our customers. Working closely with our customers on their core technologies that implement our solutions, with a common focus on their business results, provides direct and real-time feedback for continual improvement of our solutions. We believe that we will generate expanded relationships with customers that engage us on terms that include a significant gainshare performance incentive component.

Focus on Key IC Product Segments and High-Growth Adjacent Markets. We intend to focus our solutions on high-volume, high-growth IC product segments such as system-on-a-chip, memory, CMOS image sensor, and high-performance central processing units. As a result, we will continue to expand our solutions for technology drivers such as low-k dielectrics, high-k metal gates, immersion lithography, double patterning, SOI, Finfets, copper, and 300mm wafer fabs, which are all still somewhat new or are relatively complex manufacturing technologies. We believe that these product segments are particularly attractive because they include complex IC design and manufacturing processes where processed silicon is costly and yield is critical. In addition, we have expanded our efforts to penetrate relatively new and potentially high-growth adjacent markets, such as photovoltaic and LED manufacturing, and we are leveraging our yield management system and FDC technology to create products that meet the needs of these markets.

Expand Strategic Relationships. We intend to continue to extend and enhance our relationships with companies at various stages of the design-to-silicon process, such as process licensors, manufacturing and test equipment vendors, electronic design automation vendors, silicon IP providers, semiconductor foundries, and contract test and assembly houses.

PDF Solutions was incorporated in Pennsylvania in November 1992. We reincorporated in California in November 1995 and reincorporated in Delaware in July 2000. In July 2001, the company completed an initial public offering and our shares of common stock are currently traded on the NASDAQ. Headquartered in San Jose, California, PDF Solutions operates worldwide with additional offices in China, Europe, Japan, Korea, Singapore, and Taiwan.

Industry Background

Rapid technological innovation, with increasingly shorter product life cycles, now fuels the economic growth of the semiconductor industry. IC companies historically ramped production slowly, produced at high volume once products

gained market acceptance, and slowly reduced production volume when price and demand started to decrease near the end of the products' life cycles. Now, companies often need to be the first to market and the first to sell the most volume when a product is first introduced so that they have performance and pricing advantages over their competition, or else they lose market opportunity and revenue. Increased IC complexity and compressed product lifecycles create significant challenges to achieve competitive initial yields and optimized performance. For example, it is not uncommon for an initial manufacturing run to yield only 20%, which means that 80% of the ICs produced are wasted. Yield improvement and performance optimization are critical drivers of IC companies' financial results because they typically lead to cost reduction and revenue generation concurrently, causing a leveraged effect on profitability.

Technology and Intellectual Property Protection

We have developed proprietary technologies for yield simulation, analysis, loss detection, and improvement. The foundation for many of our solutions is our CV infrastructure ("CVi") that enables our customers to characterize the manufacturing process, and establish fail-rate information needed to calibrate manufacturing yield models, prioritize yield improvement activities and speed-up process learning-cycles. Our CVi includes proprietary Characterization Vehicle® test chips, including designs of experiments and layout designs, and a proprietary and patented highly parallel electrical functional and parametric-test system, comprised of hardware and software designed to provide an order-of-magnitude reduction in the time required to test our Characterization Vehicle® test chips. In addition, our technology embodies many algorithms, which we have developed over the course of many years, and which are implemented in our products including dataPOWER®, pdCVtm, mæstria®, and pdBRIXtm, among others. Further, our IP includes methodologies that our implementation teams use as guidelines to drive our customers' use of our CV® test chips and technologies, quantify the yield-loss associated with each process module and design block, simulate the impact of changes to the design and/or to the manufacturing process, and analyze the outcome of executing such changes. We continually enhance our core technologies through the codification of knowledge that we gain in our solution implementations.

Our future success and competitive position rely to some extent upon our ability to protect these proprietary technologies and IP, and to prevent competitors from using our systems, methods, and technologies in their products. To accomplish this, we rely primarily on a combination of contractual provisions, confidentiality procedures, trade secrets, and patent, copyright, mask work, and trademark laws. We license our products and technologies pursuant to non-exclusive license agreements that impose restrictions on customers' use. In addition, we seek to avoid disclosure of our trade secrets, including requiring employees, customers, and others with access to our proprietary information to execute confidentiality agreements with us and restricting access to our source code. We also seek to protect our software, documentation, and other written materials under trade secret and copyright laws. As of December 31, 2011, we held 60 U.S. patents. We intend to prepare additional patent applications when we feel it is beneficial. Characterization Vehicle®, Circuit Surfer®, CV®, dataPOWER®, mæstria®, ModelWare®, pdFasTest®, PDF Solutions®, the PDF Solutions logo, Yield Ramp Simulator®, and YRS® are registered trademarks of PDF Solutions, Inc. or its subsidiaries, and Design-to-Silicon-Yieldtm, dataPOWER® VSF™, dP-bitMAPtm, dP-Defecttm, dP-Miningtm, dP-SSAtm, dP-Variability Analysis™, dP-WorkFlow™, exensio™, pdBRIXtm, pdCVtm, Template™, exensi and YA-FDC™ are our common law trademarks.

Products and Services

Our solutions consist of integration engineering services, proprietary software, and other technologies designed to address our customers' specific manufacturing and design issues.

Services and Solutions

Manufacturing Process Solutions ("MPS"). The IC manufacturing process typically involves four sequential phases: research and development to establish unit manufacturing processes, such as units for the metal CMP or lithography processes; integration of these unit processes into functional modules, such as metal or contact modules; a yield ramp of lead products through the entire manufacturing line; and volume manufacturing of all products through the life of the process. We offer solutions targeted to each of these phases designed to accelerate the efficiency of yield learning by shortening the learning cycle, learning more per cycle, and reducing the number of silicon wafers required. Our targeted offerings include:

- Process R&D: Our process R&D solutions are designed to help customers increase the robustness of their manufacturing processes by characterizing and reducing the variability of unit processes and device performance with respect to layout characteristics within anticipated process design rules.

- Process Integration and Yield Ramp: Our process integration and yield ramp solutions are designed to enable our customers to more quickly ramp the yield of new products early in the manufacturing process by characterizing the process-design interactions within each key process module, simulating product yield loss by process module, and prioritizing quantitative yield improvement by design block in real products.

Volume Manufacturing Solutions ("VMS"). Our volume manufacturing solutions are designed to enable our customers to extend our yield ramp services through the life of the process by continuing to collect test data and equipment signals during production and improving yield while reducing the overhead of manufacturing separate test wafers. Our dataPOWER® VSF™ software allows customers to perform rapid yield signature detection, characterization, and diagnosis. Our mæstria® and YA-FDC™ process control software offerings enable our customers to monitor and control process signals to detect and diagnose yield loss related to equipment performance. Our exensio™ software suite, which comprises our dataPOWER® VSF™, mæstria® and YA-FDC™ tools, enables customers to collect and combine product test data and equipment signals during production to improve yield while simultaneously reducing the overhead of manufacturing.

Design-for-Manufacturability ("DFM") Solutions. Our DFM solutions are designed to enable our customers to optimize yields, improve parametric performance, and reduce product ramp time by integrating manufacturability considerations into the design cycle before a design is sent to the mask shop to more quickly and cost-effectively manufacture IC products. We target these solutions to customers' requirements by providing the following:

- Logic DFM Solutions: Logic DFM solutions include software, IP, CV® infrastructure, and services designed to validate customers' process design kit (PDK) and to maximize functional and parametric yield improvements while achieving requirements for density or performance, for example, in the logic portions of an IC design. A CV® optimized to the design style of an IC design provides any necessary design-specific parametric and functional yield models for the design style. Our software helps designers optimize the yield of the logic portion by using process-specific and design style-specific yield models and technology files that enable identification & implementation of IP design building block improvements that result in enhanced yield.

- Circuit Level DFM Solutions: Circuit level DFM solutions include software and services designed to anticipate the effects of process variability during analog/mixed signal/RF circuit design to optimize the manufacturability of each block given a pre-characterized manufacturing process.

- Memory DFM Solutions: Memory DFM solutions include software and services designed to optimize the memory redundancy and bit cell usage given a pre-characterized manufacturing process.

- pdBRIXtm Physical IP Solutions: pdBRIXtm physical IP solutions include software, IP, CV® infrastructure and services for identifying and developing a set of layout patterns that are optimized to a given manufacturing process and target product application. A complete characterization of all transistor and layout patterns used in these Template™ layouts can be performed with the CV® infrastructure. These Template™ layouts serve as the building blocks for design organizations to construct standard cell libraries and larger physical IP blocks, which we refer to as Bricks. This solution includes mapping software for inserting these Bricks into a design flow.

Products

Our Manufacturing Process, Volume Manufacturing, and DFM solutions incorporate the use of various elements of our software products and other technologies, depending on the customers' needs. Our software products and other technologies include the following:

Characterization Vehicle® Infrastructure. Our test chip design engineers develop a design of experiments ("DOEs") to determine how IC design building blocks interact with the manufacturing process. Our CV® software utilizes the DOE, as well as a library of building blocks that we know has potential yield and performance impact, to generate CV® test chip layouts. Our CV® infrastructure includes:

- CV® Test Chips. Our family of proprietary test chip products is run through the manufacturing process with intentional process modifications to explore the effects of potential process improvements given natural manufacturing variations. Our custom-designed CV test chips are optimized for our test hardware and analysis software and include DOEs tuned to each customer's process. Our full-reticle short-flow CV® test chips provide a fast learning cycle for specific process modules and are fully integrated with third-party failure analysis and inspection tools for complete diagnosis to root cause. Our Scribe CV® products are inserted directly on customers' product wafers and collect data from product wafers about critical layers.

- pdCVtm Analysis Software. Our proprietary software accumulates data from our CV® test chips, enabling models of the performance effects of process variations on these design building blocks to be generated for use with our Yield Ramp Simulator software.

- pdFasTest® Electrical Wafer Test System. Our proprietary system enables fast defect and parametric characterization of manufacturing processes. This automated system provides parallel functional testing, thus minimizing the time required to perform millions of electrical measurements to test our CV® test chips.

Yield Ramp Simulator® (YRS®) Software. Our YRS software analyzes an IC design to compute its systematic and random yield loss. YRS software allows design attribute extraction and feature-based yield modeling. YRS® software takes as input a layout that is typically in industry standard format and proprietary yield models generated by running and testing our CV® test chips. YRS® software is designed to estimate the yield loss due to optical proximity effects,

etch micro-loading, dishing in CMP, and other basic process issues.

Circuit Surfer® Software. Our Circuit Surfer software estimates the parametric performance yield and manufacturability of analog/mixed-signal/RF blocks in a design, such as RF transmission, PLLs/DLLs and logic critical paths. Using our Circuit Surfer software, a design engineer is able to estimate how manufacturing process variations will impact circuit performance and yield and then optimizes the circuit to reduce or eliminate the impact of those variations.

pdBRIX™ Platform. Our pdBRIX™ platform includes software for identifying and developing a set of physical IP building blocks that are tailored to a given manufacturing process and target product application. This platform also includes mapper software for inserting these physical IP building blocks into a traditional design flow.

dataPOWER® YMS Platform. Our dataPOWER® YMS platform collects yield data, loads and stores it in an integrated database and allows product engineers to identify and analyze production yield issues. Our YMS platform is designed to handle very large data sets, to efficiently improve productivity, yield and time-to-market at our customers' sites. dataPOWER® VSF™ software contains powerful visualization and reporting tools, which provide flexibility to address customers' requirements such as web-based access through the dP-Monitor™ module. dataPOWER® VSF™ Expert software additionally includes extra proprietary yield analysis software tools that aid in the diagnosis of more complex yield issues, and can be further extended through optional modules to enable defect analysis (dP-Defecttm), memory analysis (dP-bitMAPtm), spatial signature analysis (dP-SSAtm) and data-mining (dP-Miningtm).

FDC Software. Our mæstria® product provides FDC capabilities including summary indicators to rapidly identify sources of process variations and manufacturing excursions by monitoring equipment parameters through proprietary data collection and analysis features. Our ModelWare® product is a real-time FDC system for monitoring and alarming of equipment variation and manufacturing excursions.

YA-FDC™ Tools. Our YA-FDC™ software tools allow online modeling to create real-time virtual measurements of final product attributes during processing. These models enable optimization decisions for process control, process adjustments, PM scheduling, tool corrective actions, and wafer dispatching. The real-time decision-making based on the models is designed to reduce product variability and cost simultaneously. YA-FDC™ tools also enable more rapid diagnosis of yield loss mechanisms identified at the end of wafer processing through application of the developed models.

With the exception of dataPOWER® and mæstria®, the primary distribution method for our software and technologies is through our manufacturing process solutions although, we have in the past and may in the future separately license these and other technologies. Though dataPOWER® and mæstria® are primarily licensed separately, they may also be distributed within our Design-to-Silicon-Yield solutions.

Customers

Our current customers are foundries, integrated device manufacturers ("IDMs"), and fabless semiconductor design companies. Our customers' targeted product segments vary significantly, including microprocessors, memory, graphics, image sensor solutions, and communications. We believe that the adoption of our solutions by such companies for usage in a wide range of products validates the application of our Design-to-Silicon-Yield solutions to the broader semiconductor market.

Global Foundries Inc. ("Global Foundries"), International Business Machines Corporation ("IBM") and Samsung Electronics ("Samsung") represented 24%, 19%, and 15%, respectively, of our revenues for the year ended December 31, 2011. Global Foundries, Toshiba Corporation ("Toshiba"), Samsung and IBM, represented 19%, 18%, 12% and 11%, respectively, of our revenues for the year ended December 31, 2010. IBM, Toshiba, and Global Foundries represented 19%, 17%, and 11%, respectively, of our revenues for the year ended December 31, 2009. No other customer accounted for 10% or more of our revenues in 2011, 2010, and 2009.

For the year ended December 31, 2011, we derived 41% of our revenues from customers based in Asia compared to 65% for the year ended December 31, 2010 and 66% for the year ended December 31, 2009. We base these calculations on the geographic location of where the work is performed. Additional discussion regarding the risks

associated with international operations can be found under Item 1A, “Risk Factors”.

See our “Notes to Consolidated Financial Statements”, included under Part II, Item 8. “Financial Statements and Supplementary Data” for additional geographic information.

Sales and Marketing

Our sales strategy is to pursue targeted accounts through a combination of our direct sales force, our solution implementation teams, and strategic alliances. After we are engaged by a customer and early in the solution implementation, our engineers seek to establish relationships in the organization and gain an understanding of our customers’ business issues. Our direct sales and solution implementation teams combine their efforts to deepen our customer relationships by expanding our penetration across the customer’s products, processes and technologies. This close working relationship with the customer has the added benefit of helping us identify new product areas and technologies in which we should next focus our research and development efforts. We expect to continue to establish strategic alliances with process licensors, vendors in the electronic design automation software, capital equipment for IC production, silicon IP and mask-making software segments to create and take advantage of sales channel and co-marketing opportunities.

Research and Development

Our research and development focuses on developing and introducing new proprietary technologies, software products and enhancements to our existing solutions. We use a rapid-prototyping paradigm in the context of the customer engagement to achieve these goals. We have made, and expect to continue to make, substantial investments in research and development. The complexity of our Design-to-Silicon-Yield technologies requires expertise in physical IC design and layout, transistor design and semiconductor physics, semiconductor process integration, numerical algorithms, statistics and software development. We believe that our team of engineers will continue to advance our market and technological leadership. We conduct in-house training for our engineers in the technical areas, as well as focusing on ways to enhance client service skills. Although it fluctuates, we can have up to one quarter of our research and development engineers operating in the field, partnered with solution implementation engineers in a deliberate strategy to provide direct feedback between technology development and customer needs. Our research and development expenses were $14.0 million, $15.0 million and $17.9 million in 2011, 2010 and 2009, respectively.

Competition

The semiconductor industry is highly competitive and driven by rapidly changing design and process technologies, evolving standards, short product life cycles, and decreasing prices. We expect market competition to continue to develop and increase as the market for process-design integration technologies and services continues to evolve. We believe the solution to address the needs of IC companies requires a unified system of yield models, design analysis software, CV test chips, physical IP creation, process control software, and yield management software. Currently, we are the only provider of comprehensive commercial solutions for integrating design and manufacturing processes. We face indirect competition from internal groups at IC companies that use an incomplete set of components not optimized to accelerate process-design integration. Some providers of yield management software, inspection equipment, electronic design automation, or design IP may seek to broaden their product offerings and compete with us.

We face competition for some of the point applications of our solutions including some of those used by the internal groups at IC companies. Specifically there are several suppliers of yield management and/or prediction systems, such as KLA-Tencor, Mentor Graphics (through its acquisition of Ponte Solutions), Rudolph Technologies Inc. (“Rudolph”) (through its acquisition of the Yield Dynamics group), Synopsys, Inc. (“Synopsys”), and process control software, such as Applied Materials, Inc. (through its acquisition of the software division of Brooks Automation, Inc.), BISTel Inc., Rudolph, and Trancom Technology, Inc., and MKS Instruments, Inc. ARM Ltd. and Synopsys (through its acquisition of Virage Logic Corporation) provide standard cells in the physical IP space and Tela provides software for standard cell synthesis, each of which could compete with our pdBRIX™ solution. In addition, Synopsys now appears to offer directly competing DFM solutions, while other EDA suppliers provide alternative DFM solutions that may compete for the same budgetary funds.

We believe that our solutions compare favorably with respect to competition becasue we have demonstrated results and reputation, strong core technology, ability to create innovative technology, and ability to implement solutions for new technology and product generations.

Employees

As of December 31, 2011, we had 319 employees worldwide, including 203 on client service teams, 56 in research and development, 26 in sales and marketing, and 34 in general and administrative functions. Of these employees, 146 are located in the US, 126 in Asia, and 47 in Europe. Worldwide, we had 292 employees as of December 31, 2010 and 306 as of December 31, 2009.

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None of our employees are represented by a labor union. Our employees in France and Italy are subject to collective bargaining agreements in those countries. We believe our relationship with our employees is good.

Executive Officers

The following table and notes set forth information about our current executive officers as of March 13, 2012.

Name	Age	Position
John K. Kibarian, Ph.D.	48	President, Chief Executive Officer, and Director
Gregory Walker	58	Vice President, Finance and Chief Financial Officer
Michael Shahbazian	65	Vice President
Cees Hartgring, Ph.D.	58	Vice President, Client Services and Sales
Kimon Michaels, Ph.D.	45	Vice President, Products and Solutions

John K. Kibarian, Ph.D., one of our founders, has served as President since November 1991 and has served as our Chief Executive Officer since July 2000. Dr. Kibarian has served as a director since December 1992. Dr. Kibarian received a B.S. in Electrical Engineering, an M.S. E.C.E. and a Ph.D. E.C.E. from Carnegie Mellon University.

Gregory Walker has served as a Chief Financial Officer and Vice President, Finance since November 2011. Prior to joining the Company, Mr. Walker served as Sr. Vice President and Chief Financial Officer at InnoPath Software since 2007. Prior to that, Mr. Walker served as Sr. Vice President & Chief Financial Officer of Magma Design Automation, Inc. from 2002 through 2007. Earlier in his career, he held various financial roles at technology companies, including Synopsys, Inc., Integrated Device Technology, Inc., International Business Machines Corporation and Xerox Corporation. Mr. Walker received an M.B.A. from the University of Rochester in Rochester, New York and a B.A. in economics and history from Union College in Schenectady, New York.

Michael Shahbazian has served as Vice President since March 2012. Prior to this appointment, Mr. Shahbazian previously served as the Company's Interim CFO, Vice President, Finance from June 2011 through December 2011. Prior to that, Mr. Shahbazian served as chief financial officer and either senior vice president or vice president at various companies, including Guidewire Software, Inc. from November 2007 to July 2009, Embarcadero Technologies from October 2005 through July 2007, Niku Corporation (acquired by Computer Associates) from January 2003 to August 2005, ANDA Networks, Inc. from November 2000 to November 2002, Inventa Technologies, Inc. from January 2000 to November 2000, and Walker Interactive Systems, Inc. from April 1999 to January 2000. Prior to these roles, Mr. Shahbazian spent nearly 20 years with Amdahl Corporation in a variety of senior financial positions. Mr. Shahbazian holds a B.S. in Business from California State University, Fresno, and an MBA from the University of Southern California, Los Angeles, California.

Cees Hartgring, Ph.D., has served as Vice President, Client Services and Sales since June 2007. Dr. Hartgring served as Vice President and General Manager, Manufacturing Process Solutions from January 2004 through May 2007, as Vice President, Worldwide Sales and Strategic Business Development from April 2003 through December 2003 and as Vice President of Sales from September 2002 through March 2003. Prior to joining PDF, Dr. Hartgring served as President and Chief Executive Officer of Trimedia Technologies, a Philips Semiconductor spinout. Dr. Hartgring also held various executive positions at Philips Semiconductor, most recently as Vice President and General Manager of the Trimedia business unit. Dr. Hartgring received an undergraduate degree from the Technical University Delft and an M.S.E.E. and a Ph.D. in Electrical Engineering and Computer Science from the University of California at Berkeley.

Kimon Michaels, Ph.D., one of our founders, has served as Vice President, Products and Solutions since July 2010. Mr. Michaels served as Vice President, Design for Manufacturability from June 2007 through June 2010. Prior to that,

Dr. Michaels served as Vice President, Field Operations for Manufacturing Process Solutions from January 2006 through May 2007, and has been a Director since November 1995. From March 1993 through December 2005, he served in various vice presidential capacities. He also served as Chief Financial Officer from November 1995 to July 1998. Dr. Michaels received a B.S. in Electrical Engineering, an M.S. E.C.E. and a Ph.D. E.C.E. from Carnegie Mellon University.

Available Information

We file or furnish various reports, such as registration statements, periodic and current reports, proxy statements and other materials with the SEC. Our Internet website address is www.pdf.com. You may obtain, free of charge on our website, copies of our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, and amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Exchange Act, as soon as reasonably practicable after we electronically file such material with, or furnish it to, the SEC. The Company's website address provided is not intended to function as a hyperlink, and the information on the Company's website is not, and should not be considered, part of this Annual Report on Form 10-K and is not incorporated by reference herein.

In addition to the materials that are posted on our website, you may read and copy any materials we file with the SEC at the SEC’s Public Reference Room at 100 F Street, NE, Washington, DC 20549-0120. You may obtain information on the operation of the Public Reference Room by calling the SEC at 1-800-SEC-0330. The SEC also maintains a Web site (http://www.sec.gov) that contains reports, proxy and information statements and other information regarding issuers, such as us, that file electronically with the SEC.

Item 1A. Risk Factors.

It typically takes us a long time to sell our unique solutions to new customers and into new markets, and that can result in uncertainty and delays in generating revenues.

Our gainshare performance incentives business model is unique and our Design-to-Silicon-Yield solutions are often unfamiliar to new customers. This results in a long sales cycle and requires a significant amount of our senior management's time and effort. Furthermore, we need to target those individuals within a customer's organization who have overall responsibility for the profitability of an integrated circuit ("IC"). These individuals tend to be senior management or executive officers. We may face difficulty identifying and establishing contact with such individuals. Even after initial acceptance, due to the complexity of structuring the gainshare performance incentives component, the negotiation and documentation processes can be lengthy. It can take nine months or more to reach a signed contract with a customer. Unexpected delays in our sales cycle could cause our revenues to fall short of expectations. Our efforts to leverage our FDC technology in the relatively new market of the solar panel industry may not be successful. Further, ongoing negotiations and evaluation projects with photovoltaic manufacturers may not result in significant revenues for us if we are unable to close new engagements in these markets on terms favorable to us, in a timely manner, or at all, or if we are unable to successfully deliver our products and services to such markets.

We generate a large percentage of our revenues from a limited number of customers, so decreased volumes at any one of these customers, or the loss of any one of these customers could significantly reduce our revenue and results of operations below expectations.

Historically, we have had a small number of large customers for our core Design-to-Silicon-Yield solutions and we